REMARKS/ARGUMENTS

Claims 1-15 are pending in the present application. With this amendment, claims 2 and 12-13 have been amended, and claims 4, 9, and 14 have been canceled. Reconsideration of the claims is respectfully requested.

The examiner objected to the specification stating that the title was not descriptive. Applicants have amended the title. Therefore, Applicants believe this objection should be withdrawn.

The examiner objected to the specification stating that the specification failed to provide antecedent basis for the claimed subject matter. The examiner did not specifically refer to any claim in particular. The examiner referred to portions of the specification that defined the operation of a stack. Applicants' original claims 4, 9, and 14 described a stack. Applicants have canceled these claims. Applicants believe this objection has been overcome and should be withdrawn.

The specification has also been amended to correct typographical errors. No new matter has been added by any of the amendments to the specification.

The examiner objected to claims 2 and 4 because of informalities. These claims have been canceled, and this objection should be withdrawn.

I. 35 U.S.C. § 112, First Paragraph

The examiner has objected to claims 4, 9, and 14 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement specifically addressing the "stack" limitation of the claims. These claims have been canceled. Therefore, this rejection should be withdrawn.

II. 35 U.S.C. § 112, Second Paragraph

The examiner has rejected claims 12-14 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

The examiner states that these dependent claims describe an "instruction" while the independent claim describes a "line of data". Claim 14 has been canceled. Applicants have amended claims 12-13 to claim a line of data. Therefore the rejection of claims 12-14 under 35 U.S.C. § 112, second paragraph, is believed to be overcome by the amendment to the claims.

III. 35 U.S.C. § 102, Anticipation

The examiner has rejected claims 1, 3, and 6-7 under 35 U.S.C. § 102 as being anticipated by U.S. Patent Application Publication 2002/0095553 published by *Mendelson*. This rejection is respectfully traversed.

Applicants' claim 1 describes a first cache for storing a first plurality of instructions and a second cache for storing a second plurality of instructions. Each instruction of the first plurality has an associated counter. When a first instruction of the first plurality is accessed, its first associated counter is incremented.

When the first associated counter reaches a threshold, the first instruction is copied into the second cache. The first instruction is copied when the first associated counter reaches a threshold. As is clear from the claim language, the coping is not discretionary. The copying of the first instruction is required when the first associated counter reaches the threshold.

The claim also clearly defines when that required copying must occur. The first instruction is copied when the first associated counter reaches the threshold. According to claim 1, the copying occurs at the time the counter merely reaches the threshold. Thus, copying occurs prior to the counter exceeding the threshold.

Mendelson teaches a filter trace cache (FTC) and a main trace cache (MTC). Newly received traces are placed in the FTC. At a later time, a trace may be, but is not required to be, evicted from the FTC. At that time, the evicted trace will either be discarded or moved to the MTC. The decision as to whether to discard a trace or move it to the MTC will depend on that trace's access counter value. If the value is below a threshold, the trace is discarded. If the value is equal to or above a threshold, the trace is moved to the MTC.

Traces can stay in the FTC indefinitely regardless of their counter value. Traces stay as long as new traces do not evict them. See page 3, paragraph 0033. Thus, a trace stays in the FTC until a new trace is received that must replace the existing trace. If, for example, a trace is in the FTC and no new traces are received, that existing trace will stay in the FTC.

A trace will stay in the FTC regardless of its counter value. Thus, the trace in the example above where no new traces are received will stay in the FTC while its counter value continues to increase well beyond the threshold value. A trace is only evicted from the FTC when a new trace needs to be stored in the existing trace's location. Only when a new trace is received that needs to replace an existing trace is a determination made as to whether to discard the existing trace or to move the existing trace to the MTC.

Traces are not moved out of the FTC because their values reached a threshold. Traces can stay in the FTC even after their counter values reached a threshold. Traces are moved out only because a new trace will be stored in the existing trace's location in the cache.

A decision as to whether to discard the existing trace or move the existing trace requires evaluating the counter. This decision is only made once an existing trace is evicted. This decision is not made prior to the trace being evicted. Prior to the trace being evicted, the trace remains in the FTC regardless of the counter value. The counter can continue to increase indefinitely, well beyond the threshold.

No action is taken to move a trace out of the FTC based on the trace's counter value. A trace is only moved out of the FTC when that trace is evicted by a new trace. The counter value plays no part in the decision as to whether or not a trace will be evicted.

Applicants' claim 1 describes "when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache". Thus, according to Applicants' claim, the first instruction is copied when the counter reaches a threshold. No other action is involved in the decision to copy an instruction. When the counter reaches the threshold, the first instruction is copied. Unlike *Mendelson* where traces can stay in the FTC after their counter value reaches a threshold, according to Applicants' claims, the first instruction cannot stay in the first cache once its counter reaches a threshold. The first instruction must be copied once its counter reaches the threshold.

Mendelson does not teach a trace being copied when its value reaches a threshold. In *Mendelson*, a trace can remain in the FTC with its value well above the threshold. Therefore, *Mendelson* does not teach when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache. Therefore, *Mendelson* does not anticipate Applicant's claim 1.

Applicants' claim 3 depends from claim 1. Because *Mendelson* does not anticipate claim 1, *Mendelson* does not anticipate claim 3.

Applicants' claim 6 describes if the first associated counter exceeds the threshold, moving the first instruction from the first cache to a second cache. Similarly to claim 1, moving the first instruction is not discretionary. The first instruction is moved if the first associated counter exceeds the threshold.

As discussed above, *Mendelson* teaches a cache, the FTC, in which a trace can remain indefinitely while its value far exceeds the threshold. Traces are not moved out of the FTC because their values exceeded a threshold. Traces are moved out because a new trace will be stored in the existing trace's location in the cache. The trace's counter value is used to determine whether that trace, which is about to be overwritten, will be overwritten (and essentially discarded) or whether that trace will be moved to the MTC. The trace is not moved because its counter value exceeded the threshold. The trace is either discarded or moved because another trace is about to overwrite the existing trace.

According to Applicants' claims, the first instruction is moved if the counter exceeds the threshold. This is mandatory according to Applicants' claims.

Mendelson does not teach a trace being copied when its value exceeds a threshold. In *Mendelson*, a trace can remain in the FTC even after its value far exceeds the threshold. Therefore, *Mendelson* does not teach if the first associated counter exceeds the threshold, moving the first instruction from the first cache to a second cache. Therefore, *Mendelson* does not anticipate Applicants' claim 6.

Applicants' claim 7 depends on claim 6. Because *Mendelson* does not anticipate claim 6, *Mendelson* does not anticipate claim 7.

IV. 35 U.S.C. § 103, Obviousness

The examiner has rejected claims 2 and 8 under 35 U.S.C. § 103 as being unpatentable over *Mendelson* in view of U.S. Patent Application Publication 2001/0001873 published by *Wickeraad*. This rejection is respectfully traversed.

Claims 2 and 8 describe similar features. These claims describe wherein each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second plurality are decremented.

The examiner relies on *Wickeraad* to cure the deficiencies of *Mendelson*. *Wickeraad*, however, does not cure the deficiencies of *Mendelson*. The combination does not render these claims unpatentable because the combination does not describe, teach, or suggest the combination of wherein when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache, wherein each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second plurality are decremented.

The examiner has rejected claims 5 and 10 under 35 U.S.C. § 103 as being unpatentable over *Mendelson* in view of Norman P. Jouppi, Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers [*Jouppi*]. This rejection is respectfully traversed.

Claims 5 and 10 describe similar features. These claims describe the first cache being an instruction cache and the second cache being fully associative and following a least recently used policy.

The examiner relies on *Jouppi* to cure the deficiencies of *Mendelson*. *Jouppi*, however, does not cure the deficiencies of *Mendelson*. The combination does not render these claims unpatentable because the combination does not describe, teach, or suggest the combination of wherein when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache and the first cache being an instruction cache and the second cache being fully associative and following a least recently used policy.

The examiner has rejected claims 11-12 under 35 U.S.C. § 103 as being unpatentable over *Mendelson* in view of Andrew S. Tannenbaum, Structured Computer Organization [*Tannenbaum*]. This rejection is respectfully traversed.

Claim 11 describes fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache.

The examiner relies on *Tannenbaum* to cure the deficiencies of *Mendelson*. *Tannenbaum*, however, does not cure the deficiencies of *Mendelson*. The combination does not render these claims unpatentable because the combination does not describe, teach, or suggest fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache.

Claim 12 depends from claim 11 and is believed patentable for these reasons given above.

The examiner has rejected claim 13 under 35 U.S.C. § 103 as being unpatentable over *Mendelson* in view of *Tannenbaum* and further in view of *Wickeraad*. This rejection is respectfully traversed.

Claim 13 describes wherein each line of data of the second cache has an associated counter, and wherein when a line of data of the second cache is accessed, all other counters of the second cache are decremented.

The examiner relies on the combination of *Tannenbaum* and *Wickeraad* to cure the deficiencies of *Mendelson*. The combination of *Tannenbaum* and *Wickeraad*, however, does not cure the deficiencies of *Mendelson*. The combination does not render these claims unpatentable because the combination does not describe, teach, or suggest the combination of fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache and wherein each line of data of the second cache has an associated counter, and wherein when a line of data of the second cache is accessed, all other counters of the second cache are decremented.

The examiner has rejected claim 15 under 35 U.S.C. § 103 as being unpatentable over *Mendelson* in view of *Tannenbaum* and further in view of *Jouppi*. This rejection is respectfully traversed.

Claim 15 describes wherein the first cache is an instruction cache and the second cache is fully associative and follows a least recently used policy.

The examiner relies on the combination of *Tannenbaum* and *Jouppi* to cure the deficiencies of *Mendelson*. The combination of *Tannenbaum* and *Jouppi*, however, does not cure the deficiencies of *Mendelson*. The combination does not render these claims unpatentable because the combination does not describe, teach, or suggest the combination of fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache and wherein the first cache is an instruction cache and the second cache is fully associative and follows a least recently used policy.

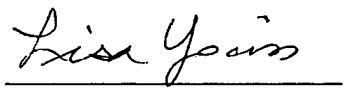
V. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 03/23/06

Respectfully submitted,



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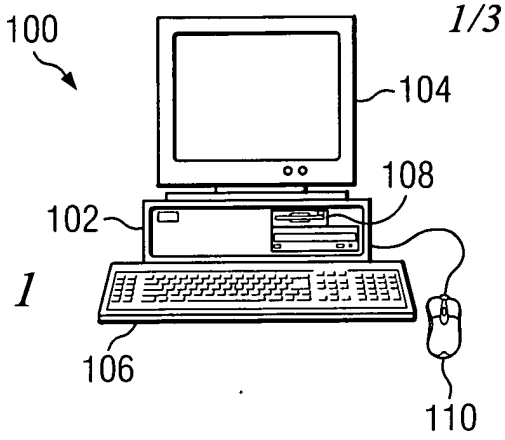

FIG. 1

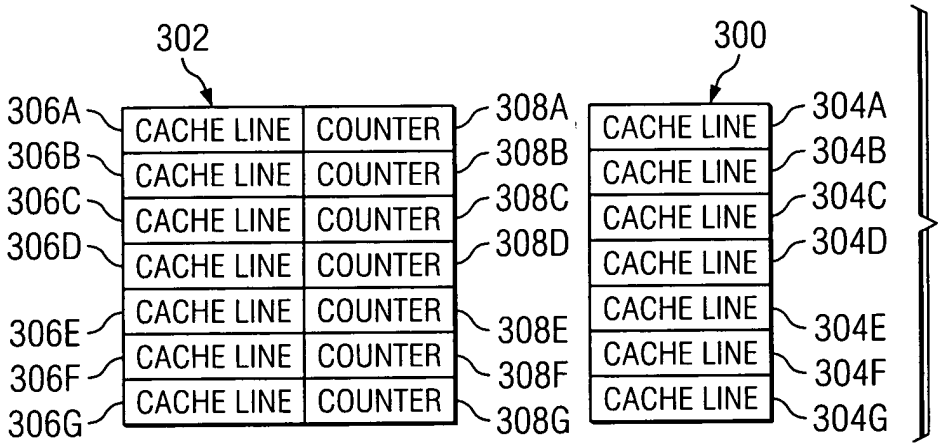

FIG. 3

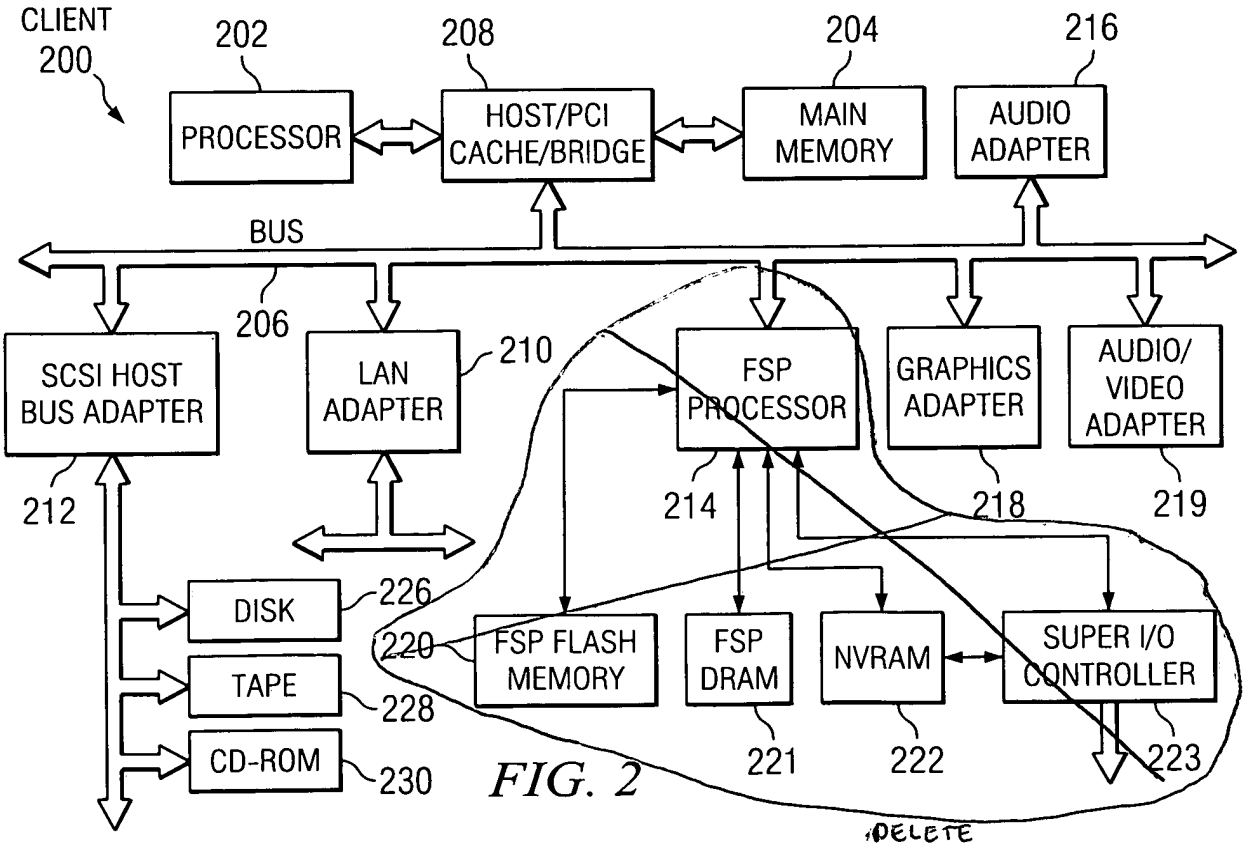

FIG. 2